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Kilovolt Tri-Gate GaN Junction HEMTs with High Thermal Stability

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***Abstract*— The lack of reports on the high-temperature performance of tri-gate GaN power HEMTs has raised serious concern on their competitiveness. This work demonstrates the first normally-off tri-gate GaN HEMT that can block kilovolts at 150 °C and zero gate bias. The key enabling device design is a new type of tri-gate, the junction tri-gate, which comprises p-n junction wrapping around AlGaN/GaN fins in the gate region. At 150 °C, the GaN tri-gate junction HEMT (Tri-JHEMT) retains strong gate control and stable threshold voltage, while the traditional tri-gate metal-insulator-semiconductor (MIS) HEMTs fabricated on the same wafer shows a large threshold voltage shift and inferior capabilities of voltage blocking. These results show the excellent thermal stability of GaN Tri-JHEMTs and their great potentials for power electronics applications.**

Keywords*— GaN, HEMT, junction gate, tri-gate, high temperature, breakdown.

I. Introduction

The GaN high electron mobility transistors (HEMT) has recently been commercialized for power electronics up to 650 V as a superior replacement of the Si counterpart, thanks to the high critical electric field of GaN and the high electron mobility of the two-dimensional electron gas (2DEG). A sufficiently positive threshold voltage (V_{TH}) is highly preferred for power devices, while the GaN HEMT is intrinsically normally-on. The normally-off technology in commercial GaN HEMTs relies on the insertion of a thick p-GaN below the gate [1]. Another popular normally-off approach is to fully recess the AlGaN barrier below gate and replace the 2DEG channel with a MOS channel [2]. However, the p-GaN gate and the MOS gate would induce a low electron concentration or a low carrier mobility in the channel, thereby compromising the device on-resistance (R_{ON}).

The 3D tri-gate and FinFET structures have been recently introduced to GaN HEMT for power and RF applications [3, 4]. Thanks to the superior gate control, the tri-gate HEMT allows for high V_{TH} with a reduced R_{on} as compared to the planar normally-off HEMTs. The tri-gate also enables superior on-off current ratio, subthreshold slope (SS), and transconductance [5,6]. Despite these advantages, current tri-gate HEMTs based on a metal-insulator-semiconductor (MIS) gate stack are still facing difficulties in achieving a high and thermally stable V_{TH}. First, a fin width down to 30 nm is often required for the realization of a positive V_{TH} [3]. Additional

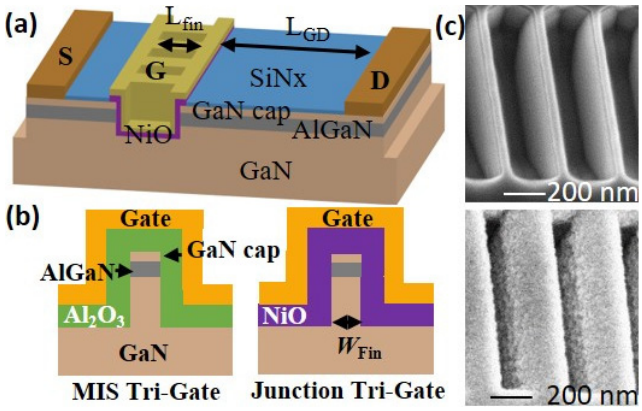

Fig. 1. (a) 3D schematic of a Tri-gate GaN junction HEMT using NiO as the p-type junction material. (b) Fin cross-section view of a MIS tri-gate (left) and a junction tri-gate (right). (c) SEM images of the 40-nm-wide AlGaN/GaN fins before and after150 nm NiO sputtering.

AlGaN recess [5] or charge trapping dielectric layers [7] have been used for relaxing the lithography requirement. However, these approaches require extra etch steps or complex dielectric structures. Second, the V_{TH} of tri-gate MISHEMTs (Tri-MISHEMTs) was found to be instable at high temperatures, making it difficult for device to remain normally-off at high temperatures [3]. In fact, there has been no literature report on the demonstration of a normally-off Tri-MISHEMT that can block high voltage at elevated temperatures such as 150 °C, a temperature that any commercial power device should be able to operate reliably for a long time. This gap has become a serious concern for the true prospects of tri-gate GaN HEMTs to reach the commercialization with a superior performance over the planar p-gate GaN HEMTs.

In this work, we used a distinct tri-gate device concept, the tri-gate junction HEMT (Tri-JHEMT), to achieve the normally-off operation and kilovolts blocking in GaN tri-gate HEMTs at high temperatures. This device concept was first proposed in [8], which utilizes p-type NiO to form a heterogenous p-n junction wrapping around the AlGaN/GaN fins in the gate region. In this work, we presented the high-temperature performance of the GaN Tri-JHEMTs and Tri-MISHEMTs fabricated on the same wafer. As compared to the MIS tri-gate, the junction tri-gate exhibited stronger gate control and superior thermal stability. The GaN Tri-JHEMT

*The two authors contribute equally to this work.

shows a breakdown voltage (*BV*) over 1.9 kV at 150 °C and zero gate voltage (V_G), which is the first normally-off kilovolt tri-gate GaN HEMT operational at 150 ºC to date.

II. Experiment

The Tri-JHEMTs are fabricated on a 6-inch GaN-on-Si wafer grown by Enkris Semiconductor Inc. The epi-structure consists of a buffer layer, 420 nm i-GaN, 22 nm $Al_{0.3}Ga_{0.7}N$, 3 nm GaN cap layer and 10 nm in-situ SiN_x grown by metal-organic chemical vapor deposition. The electron density and sheet resistance are 8.5×10^{12} cm^{-2} and 480 Ω/sq, respectively.

The schematic of Tri-JHEMT is shown in Fig. 1. The fabrication flow is the same as our previous report [8]. The device fabrication starts from removing the in-situ SiN_x and depositing 40 nm SiO_2 in plasma-enhanced chemical vapor deposition (PECVD), followed by electron-beam lithography to lift-off Cr as hard mask. 140 nm fins are etched by reactive ion etching and then dipped into 5 % tetramethylammonium hydroxide (TMAH) to remove the etching damages [9]. Fig. 1 (c) shows the scanning electron microscopy (SEM) images of the fins after TMAH treatment. The SiO_2 works as a protection layer in this wet treatment. SiO_2 is then removed by BOE. Ti/Al/Ni/Au Ohmic contact is formed for source and drain.

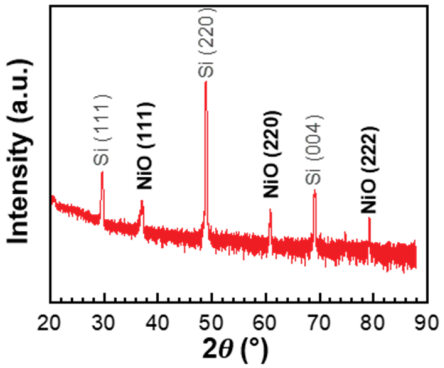

Fig. 2. XRD spectrum of the 100-nm-thick NiO sputtered on (001) Si. The corresponding crystalline planes of NiO and Si are marked on diffraction peaks. The NiO is polycrystalline.

The conformal NiO layer is deposited by magnetic sputtering at the room temperature, using the NiO target in an Ar (70%) / O_2 (30%) atmosphere. The chamber pressure is 3 mTorr and the RF power is 100 W. The NiO crystal quality is characterized by XRD (Fig. 2) showing a polycrystalline structure with a lattice constant similar to [10]. The electrical property of NiO is characterized by Hall measurement, revealing a hole concentration of 5×10^{19} cm^{-3}. The NiO thickness is 150 nm. Ni/Au is deposited on NiO as the gate, which forms Ohmic contact to NiO. PECVD SiN_x is deposited for the passivation. GaN Tri-MISHEMTs are fabricated on the same wafer using 15 nm Al_2O_3 as the gate dielectric.

III. Result and Discussion

Fig. 3 shows the transfer characteristics of Tri-JHEMTs and Tri-MISHEMTs with 21 µm gate-to-drain distance (L_{GD}), 1 µm fin length (L_{Fin}), 40 nm fin width (W_{fin}), and 150 nm fin spacing, at the temperatures of 25 ºC and 150 ºC. Tri-JHEMTs show a much smaller hysteresis and a threshold voltage shift of merely -0.19 V from 25 to 150 °C. Tri-MISHEMTs show a threshold voltage shift of over -2.5 V from 25 to 150 °C. Fig. 4 shows the output characteristics of Tri-JHEMTs and Tri-

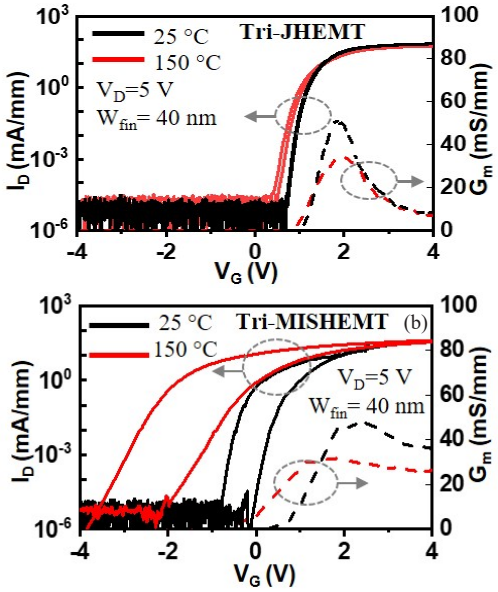

Fig. 3. Double-sweep transfer characteristics of (a) Tri-JHEMTs and (b) Tri-MISHEMTs at 25 ºC and 150 ºC. The Tri-JHEMT's threshold voltage shows small hysteresis and decreases from 0.9 V at 25 ºC to 0.71 V at 150 ºC (V_{TH} extracted at I_D=1 µA/mm). The Tri-MISHEMT's threshold voltage V_{TH} shows large hysteresis and over -2.5 V shift at 150 ºC.

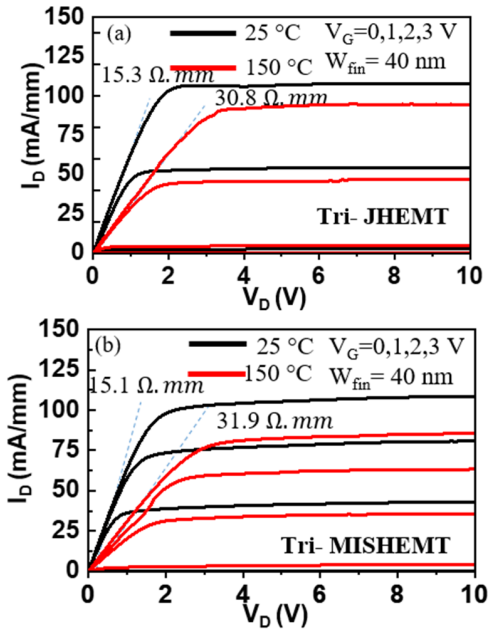

Fig. 4. Output characteristics of (a) Tri-JHEMTs and (b) MISHEMTs at 25 ºC and 150 ºC. L_{GD} is 21 µm.

MISHEMTs. The on-resistance (R_{ON}) of both devices was found to double when the temperature increases to 150 ºC.

Fig. 5 (a) shows the off-state I-V characteristics of Tri-JEHMTs with 40 nm W_{fin}. At 25 ºC, the *BV* of Tri-JHEMT was found to be over 2 kV at V_G = 0 V. At 150 ºC, the *BV* of Tri-JHEMTs retains above 1.9 kV at V_G = 0 V. The leakage current increases by around 2 orders of magnitude at 150 ºC. Fig. 5 (b) shows the off-state I-V characteristics of Tri-MISHEMTs with 40 nm W_{fin}. At 25 ºC, the Tri-MISHEMT shows similar reverse blocking capability at V_G = 0 V. At 150 ºC, Tri-MISHEMTs show punch-through at V_G = 0 V. The punch-through of Tri-MISHEMTs can be prevented by applying V_G = -5 V but the *BV* degrades to 1.3 kV. All devices

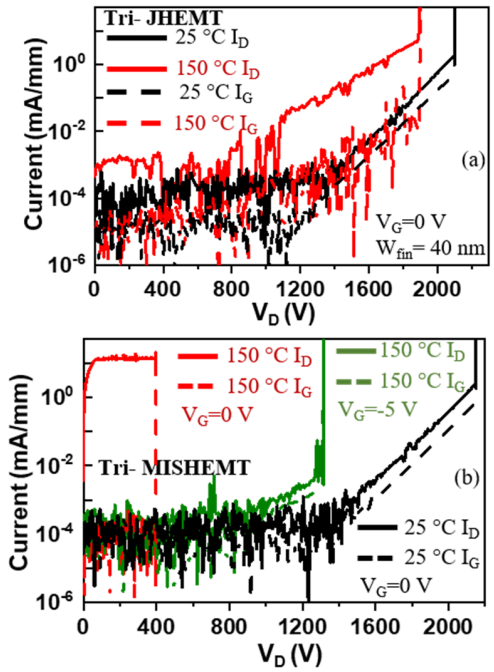

Fig. 5. (top) Off-state I_D-V_D and I_G-V_D characteristics of Tri-JHEMTs at 25 ºC and 150 ºC. V_G is 0 V. BV > 1.2 kV when substrate is grounded at 150 ºC and zero V_G. (bottom) Off-state I_D-V_D and I_G-V_D characteristics of Tri-MISHEMTs (W_{fin} = 40 nm) at 25 ºC and 150 ºC with V_G of 0 V and -5 V. At 150 ºC, the Tri-MISHEMT punches through at V_G of 0 V.

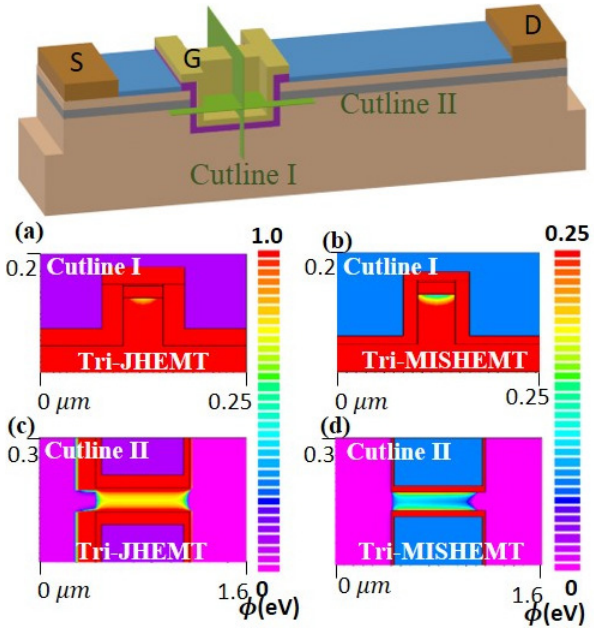

Fig. 6. TCAD simulation of the potential barrier height in the fin region. Top figure shows the simulated 3D device structure and two cutlines. (a-d) show the cross-section and top views of the potential distributions in a junction tri-gate and a MIS tri-gate with W_{fin} = 40 nm. The simulation is under V_D = 1000 V and V_G = 0 V.

in Fig. 5 (a) and Fig. 5 (b) have L_{GD} of 21 μm and are measured with the substrate floating.

The large negative shift of V_{TH} at 150 ºC in Tri-MISHEMTs is attributed to weaker sidewall control over the 2DEG. Similar phenomenon is reported for other Tri-MISHEMTs [11] and is often attributed to the sidewall interfacial traps (consistent with large hysteresis). For Tri-MISHEMTs with a small fin width, where V_{TH} is largely

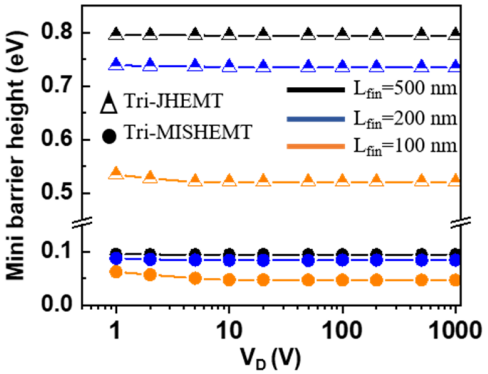

Fig. 7: Simulated minimum barrier height as function of fin length for Tri-JHEMTs and Tri-MISHEMTs at increased drain biases. The W_{fin} is 40 nm. The results suggest the feasibility of further scaling the gate length (fin length) of tri-JHEMTs while maintaining the kilovolt blocking capabilities.

controlled by sidewall depletion, such negative shift in V_{TH} at elevated temperature is more significant. This phenomenon could severely impact the application of Tri-MISHEMT at high temperatures. For Tri-JHEMTs, no similar degradation was found. The small decrease of V_{TH} for Tri-JHEMT at 150 ºC can be explained by the slightly reduced built-in potential in the NiO/GaN heterogeneous p-n junction [8].

The superior high-temperature voltage blocking capability of Tri-JHEMTs is largely benefited from the stronger gate control enabled by the absence of a gate dielectric layer and the high hole concentration in NiO. As a result, the built-in potential of the NiO/GaN heterogenous junction will all drop in GaN for depletion. This gate control capability can be further represented by the minimal potential height in the fin region (Ψ_{Fin}), which is revealed by 3D TCAD simulation in Silvaco. As shown in Fig. 6, this minimal barrier appears at the center of fin (Cutline I). Comparing the Tri-JHEMT and Tri-MISHEMT in Fig. 6, a higher Ψ_{Fin} (~0.8 eV) was found in the 40-nm junction tri-gate compared to that (~0.1 eV) in the MIS tri-gate, both at 1000 V V_D and 0 V V_G.

This higher potential height in the junction tri-gate not only ensures the voltage blocking capability at high temperatures but also allows for aggressive fin length (and gate length) scaling. Fin length (L_{fin}) is directly related to gate region resistance, but small L_{fin} could lead into Drain-induced barrier lowering (DIBL). Fig. 7 shows the simulated Ψ_{Fin} as a function of L_{fin} and drain voltage. Tri-JHEMT maintains > 0.5 eV barrier height even at a L_{fin} of 100 nm. This capability suggests the potential of Tri-JHEMTs for low-voltage devices (e.g., digital and point-of-load power applications) [8].

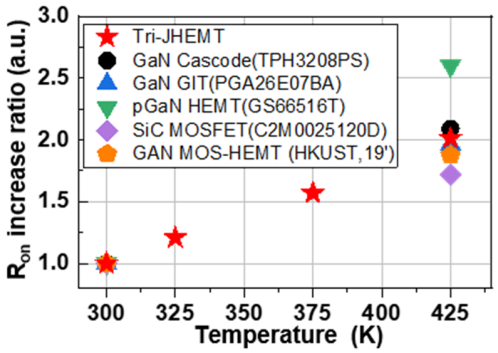

Fig. 8. Normalized R_{on} vs. temperature of Tri-JHEMTs, commercial GaN HEMTs, SiC MOSFETs, and state-of-art planar normally-off GaN MOS-HEMT [12].

TABLE I. Benchmark of drain leakage current (@80% *BV*) and *BV* at 25 ºC and 150 ºC for our Tri-JHEMTs, commercial gate injection transistors (GITs), and MOS-HEMT [12]. The GaN GIT data were from our measurement and its *BV* is defined at 8 mA current compliance.

	GaN Tri-JHEMT	**GaN GIT (igot60r070d1)**	**MOS-HEMT**
I_D **@ 80%** BV **25 °C**	6 μA/mm	9.3×10^{-6} A	10^{-4} mA/mm
I_D **@ 80%** BV **150 °C**	0.67 mA/mm	0.0017 A	N/A
$\frac{I_{D,150°C}}{I_{D,25°C}}$	113	200	N/A
BV **@ 25 °C (V)**	2120	1020	730
BV **@ 150 °C (V)**	1903	943	N/A

Fig. 8 compares the R_{ON}'s increase at 150 ºC in our Tri-JHEMTs compared to that in planar normally-off HEMTs, revealing a similar performance. TABLE I compares the *BV* and leakage current of our Tri-JHEMTs with a p-gate HEMT (gate injection transistor, GIT) and a MOS-HEMT [12]. Tri-JHEMTs show smaller leakage current increase at 150 ºC and a higher *BV* than commercial GITs (Note that no high-temperature leakage and *BV* characteristics have been reported in high-voltage MOS-HEMTs). These results manifest the excellent thermal stability of GaN Tri-JHEMTs, which benefits from the superior gate control and excellent stability of the novel junction tri-gate.

Finally, it should be noted that this NiO/GaN junction fin was recently utilized to demonstrate a GaN Schottky barrier diode (SBD) that can block ~5 kV at 150 ºC [13]. Industrial vertical GaN Fin-JFETs have shown one of the best R_{ON} v.s. *BV* trade-offs in all 1.2-kV transistors, as well as the first avalanche capability in GaN power transistors [14,15]. These high-performance devices suggest many new capabilities that the junction and fin can bring to power devices.

IV. Conclusion

We demonstrate the first high-temperature-operational tri-gate GaN HEMT with kilovolts blocking capability using the junction tri-gate technology. The NiO-GaN hetero-p-n junctions that wraps about the AlGaN/GaN fin allow for strong gate control and excellent thermal stability, enabling a Tri-JHEMT with a BV of 1.9 kV under zero V_G at 150 ºC. These results show the great potential of GaN Tri-JHEMT for power electronics applications and the wide applicability of the "junction-fin" in high-voltage GaN HEMTs and SBDs [13] for potential control and electric field management.

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